HARD PHASE ALIGNMENT OF CLOCK SIGNALS WITH AN OSCILLATOR CONTROLLER

ABSTRACT

A oscillator controller (1300, 1500) is described. Differential logic receives a clock signal and an inverted version thereof (210, 210B) and an oscillator signal and an inverted version thereof (208, 208B), where the clock signal (210) and the oscillator signal (208) having different frequencies. The differential logic provides a differential output (1611, 1612) at least partially responsive to at least one of the clock signal and the oscillator signal. The differential logic is a combinational circuit in an oscillator alignment state and a sequential circuit in a hard-phase alignment state. Control signals (1317, 1318) are used in part to selectively alternate between putting the differential logic in the oscillator alignment state and in the hard-phase alignment state.